	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition	Error
1	BRS	L1	2	"20010021524"	USPAT; US-PGPUB; EPO; JPO; DERWENT;	2003/08/07 13:01			0
2	BRS	L2	20	"5569948"	USPAT; US-PGPUB; EPO; JPO; DERWENT;	2003/08/07 13:01			0
3	BRS	L3	16	"6080620"	USPAT; US-PGPUB; EPO; JPO; DERWENT;	2003/08/07 13:01			0
4	BRS	L4	8	"6150213"	USPAT; US-PGPUB; EPO; JPO; DERWENT;	2003/08/07 13:01			0
5	BRS	L5	3	"6410390"	USPAT; US-PGPUB; EPO; JPO; DERWENT;	2003/08/07 13:01			0
6	BRS	L6	46	1 or 2 or 3 or 4 or 5	USPAT; US-PGPUB; EPO; JPO; DERWENT;	2003/08/07 13:02			0
7	BRS	L7	41	6 and (plug or inner or outer or spacers or conductive)	USPAT; US-PGPUB; EPO; JPO; DERWENT;	2003/08/07 13:03			0

US PAT NO: **5,858,865** [IMAGE AVAILABLE] L2: 1 of 1

SUMMARY:

BSUM(7)

According . . . of the wafer and flowed or densified to fill the surface features of the wafer. The BPSG forms a dielectric **planarization** layer. Upon the resulting relatively flat BPSG surface, a plug mask in the form of a patterned photoresist layer is. . .

SUMMARY:

BSUM(16)

CMP . . . self-aligned with the nitride-enclosed gate structures. Second, a major goal of CMP or dry etch-back is to provide a precisely **planarized** surface for subsequent processing steps. CMP to the second depth improves the flatness of the polished surface above that of. . .

DETDESC:

DETD(21)

FIG. . . . 362 having relatively larger landing pads than possible with previously known processes, but does not take advantage of the more **planar** nature of the top surface possible with CMP down to the level of nitride 328.

CLAIMS:

CLMS(1)

What . . .
regions, said facets being formed on said dielectric enclosure layer at the top corners of said gate stacks;
producing a dielectric **planarization** layer over said substrate and all structures thereon;
selectively removing said dielectric **planarization** layer at least over one of said contact regions;
depositing a layer of conducting material to contact at least one of. . . over the substrate from the top down to a depth at least as low as a top of said dielectric **planarization** layer, said depth being selected to provide that said layer of conductive material remains in contact with at least one. . .

CLAIMS:

CLMS(10)

10. . . . sides, each of said gate stacks being enclosed in a silicon nitride enclosure layer, said method comprising:
producing a BPSG **planarization** layer over said substrate and all structures thereon;
selectively removing said BPSG **planarization** layer over at least one of said contact regions and etching said silicon nitride enclosure layer to form facets thereon. . . over the substrate from the top down to a depth at least as low as a top of said dielectric

planarization layer.

CLAIMS:

CLMS(13)

13. . . . convergence of said top and said sides, said method comprising:
etching said shoulder region to form a facet;
producing a dielectric **planarization** layer over said substrate;
providing a patterned photoresist layer upon said dielectric **planarization** layer;
isotropically etching said dielectric **planarization** layer to remove said dielectric **planarization** layer and expose said contact regions, wherein a stack of said dielectric **planarization** layer extends from the top of each said dielectric enclosure layer;
depositing a layer of conducting material to contact said contact. . . material deposited over the substrate to isolate the conducting material above the substrate between each said stack of said dielectric **planarization** layer extending from the top of said dielectric

US PAT NO: **5,387,550** [IMAGE AVAILABLE] L9: 1 of 1

ABSTRACT:
A . . . electrical connection between the tungsten plug and the aluminum line. The poly fillet is formed by a poly deposit and **planarization** performed between a tungsten plug overetch and aluminum line deposition.

SUMMARY:

BSUM(15)

The . . . and smooths out the irregular surface of the tungsten plug. Preferably, the deposition of the poly layer is followed by **planarizing** by either a dry etch or a chemical mechanical polish. This creates a poly fillet which makes good contact with. . .

SUMMARY:

BSUM(19)

The . . . filling the well; creating a layer of doped silicon on the wafer, thereby filling the well with the doped silicon; **planarizing** the layer of silicon to provide a poly fillet in the well, the fillet having a smooth contact surface. Preferably,. . . the step of creating comprises creating a layer of insitu doped polysilicon in an LPCVD process. Preferably, the step of **planarizing** comprises a dry etch step. Alternatively, the step of **planarizing** comprises a chemical mechanical polishing step.

DRAWING DESC:

DRWD(4)

FIG. . . . a cross-sectional view of the portion of the semiconductor device wafer of FIG. 2 after the poly fillet deposition and **planarization**; and

DETDESC:

DETD(8)

In FIG. 3 a layer of polysilicon has been deposited and **planarized** to create poly fillet 26. In the preferred embodiment, fillet 26 is composed of insitu N-doped polysilicon, although any type. . . the problems of cracking and breakage of the prior art. After the doped poly silicon has been deposited, it is **planarized**, preferably by a dry etch step or a chemical mechanical polish (CMP). Any other suitable **planarization** method may be used. The result is a smooth, **planar**

S PAT NO: **5,506,166** [IMAGE AVAILABLE] L17: 1 of 1

ABSTRACT:
The . . . plug in a thick layer of insulative material such as oxide or oxide/nitride. The conductive plug is recessed from a **planarized** top surface of the thick insulative layer. Titanium is deposited and a rapid thermal anneal is performed. The titanium reacts. . .

SUMMARY:

BSUM(16)

The . . . plug in a thick layer of insulative material such as oxide or oxide/nitride. The conductive plug is recessed from a **planarized** top surface of the thick insulative layer. A low contact resistance material if formed at the base of the recess.. . .

DRAWING DESC:

DRWD(5)

FIG. 3 is the wafer portion of FIG. 2 following the deposit of an undoped thick oxide layer and **planarization** thereof.

DRAWING DESC:

DRWD(12)

FIGS. 10A and 10B are wafer portions of FIGS. 9A and B following the **planarization** of the titanium nitride layer.

DRAWING DESC:

DRWD(14)

FIGS. 12A and 12B are the wafer portions of FIG. 11A and 11B, respectively, following the **planarization** of the platinum layer to complete the formation of the storage node.

DETDESC:

DETD(3)

Referring . . . access memory (DRAM) cell is shown following conventional local oxidation of silicon (LOCOS) or special LOCOS processing which creates substantially **planar** field oxide regions 5 (created using modified LOCOS or trench isolation processes) and future active areas 6 (those regions of. . .

DETDESC:

DETD(5)

In . . . to minimize dopant out diffusion from the oxide 40 to the doped regions of the substrate. The oxide 40 is **planarized**, preferably chemical mechanically **planarized** (CMP), in order to provide a uniform height. Optionally nitride, oxynitride or another suitable material may be deposited as the. . .

DETDESC:

DETD(6)

In . . . procedure may be used to produce a surface with a desired endpoint or thickness, which also has a polished and **planarized** surface. Such apparatus for polishing-are disclosed in U.S. Pat. Nos. 4,193,226 and 4,811,522 which are herein incorporated by reference. Another. . .

DETDESC:

DETD(7)

At . . . lines are formed by the method described in U.S. Pat. No. 5,168,073 an initial thick oxide layer is deposited and **planarized** and then overlaid with a relatively thick Si.sub.3 N.sub.4 layer which is also **planarized**. These two layers serve the same function as the oxide layer 40 and may be used in place of Oxide. . .

DETDESC:

DETD(17)

Referring to FIGS. 10A and 10B, the titanium nitride layer 75 of FIGS. 9A and 9B, respectively, is **planarized**, preferably by CMP, in order to expose at least the oxide layer 40 and in order to retain titanium nitride 75 in recesses 70 overlying the titanium silicide 67. Portions of the oxide layer 40 may be **planarized** during this step. It is important, of course to retain a sufficient depth of titanium nitride 75 in order to. . .